Readout electronics for PID systems based on Large Area Picosecond Photodetectors

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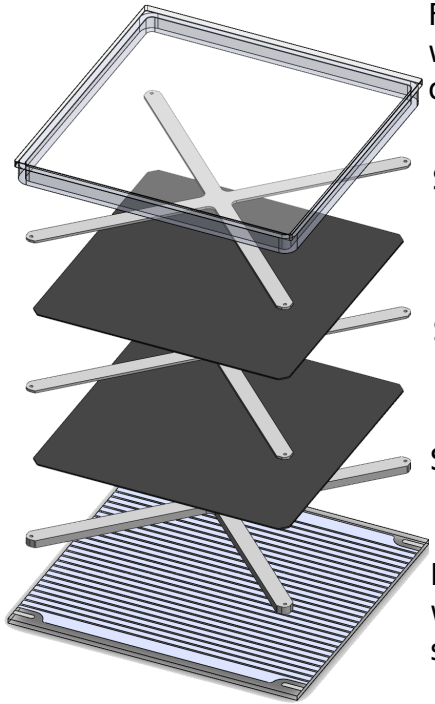
Large Area Picosecond Photodetectors (LAPPD)

INCOM BRIGHT IDEAS

- MCP based photodetector
- Large sensitive area of 200×200 mm
- Quantum efficiency $> 20\%$
- Gain $> 10^7$
- Dozen of picoseconds temporal resolution
- About 1 mm spatial resolution
- Strips anode structure



www.incomusa.com/lappd/

Stripline anode structure allows to significantly decrease number of readout channels keeping spatial resolution still high

All these features and posible feature evolution of the devices may make LAPPDs very attractivefor PID systems such as FARICH of C-Tau detector for example.

Motivation for electronics development

Motivation

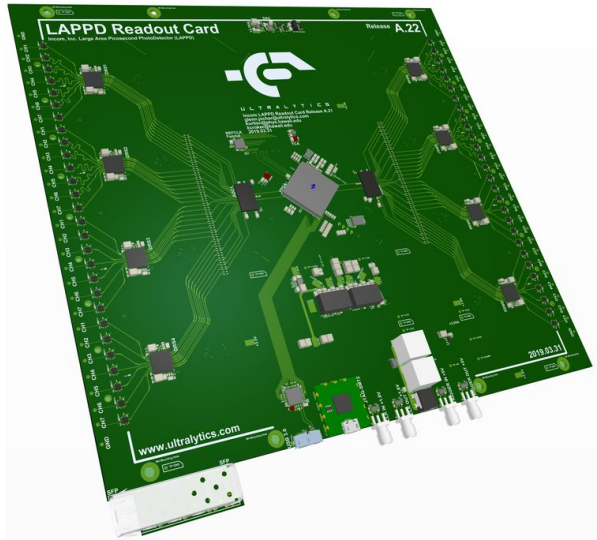
- LAPPD devices are entering early commercialization phase
- A readout card capable for work with LAPPD out of the box may be of interest for both LAPPD R&D itself and for groups who intend to use such devices for small experiments

Goals

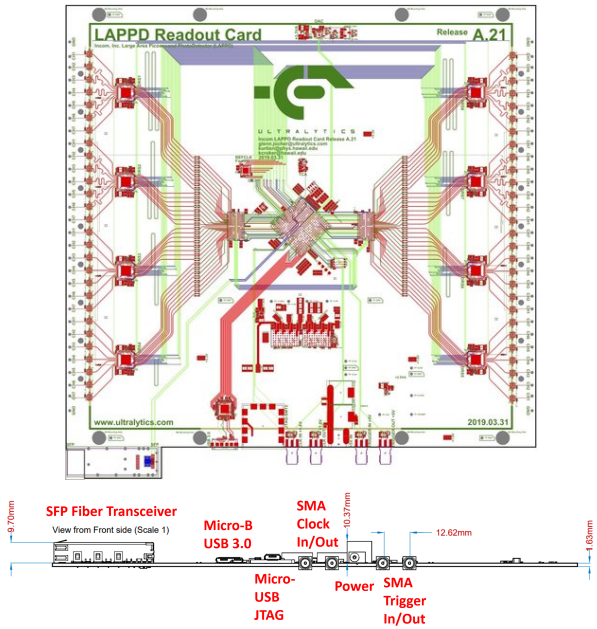
- Integrated readout solution for LAPPD photodetectors which may be easily incorporated to different experimental needs
- Parallel read out of all 56 channels of the device
- High sampling rate consistent with the LAPPD time resolution
- High speed readout
- Flexible triggering
- **Open-source** firmware/software which provides full control of the device and data taking process

LAPPD readout electronics

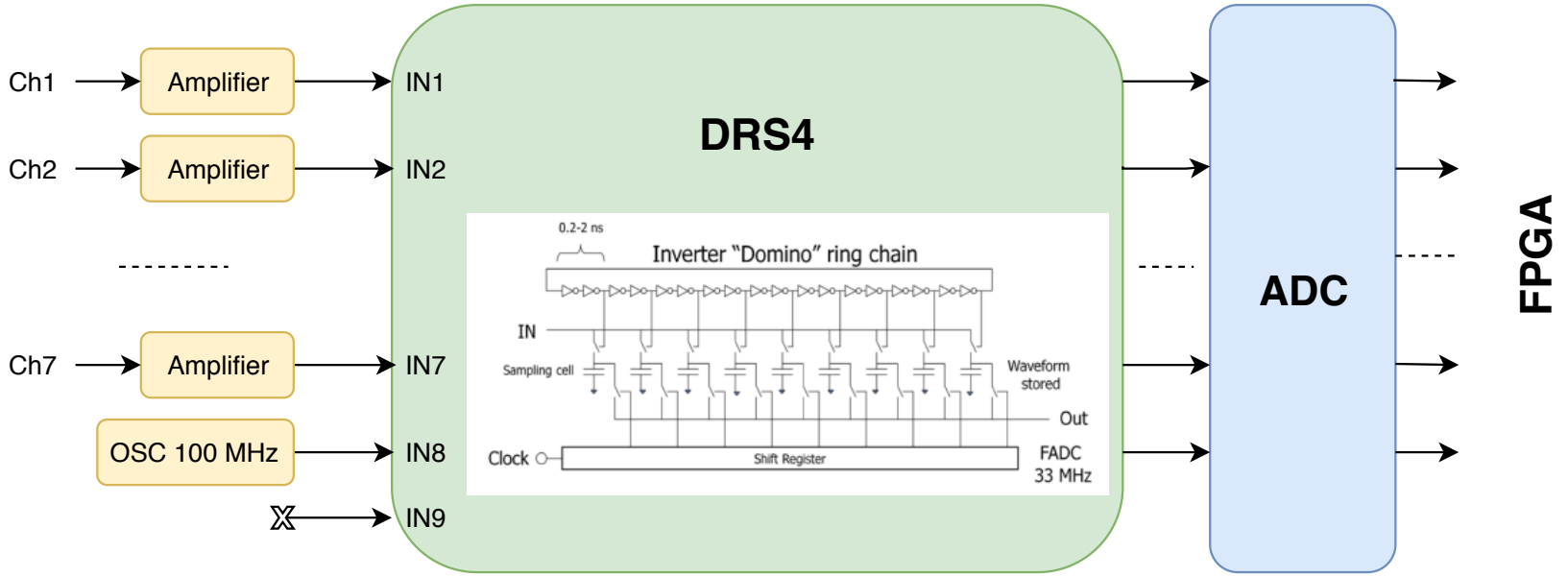
- General concept and design – cooperation of **University of Hawaii**, **Incom**, and **Ultralytics LLC**
- Hardware – **Ultralytics LLC**, Clarksburg, USA
  www.ultralytics.com/lappd
- Firmware and software – **University of Hawaii**



- Xilinx Artix-7 FPGA
- 8×DRS4 (www.psi.ch/drs)
- 2×32-channel ADS52J90 ADC for full parallel readout
- Fiberoptic transceiver
- USB 3.0, JTAG
- 4×SMA connectors for clock/trigger in/out for synchronisation among multiple boards



DRS4 for waveform sampling

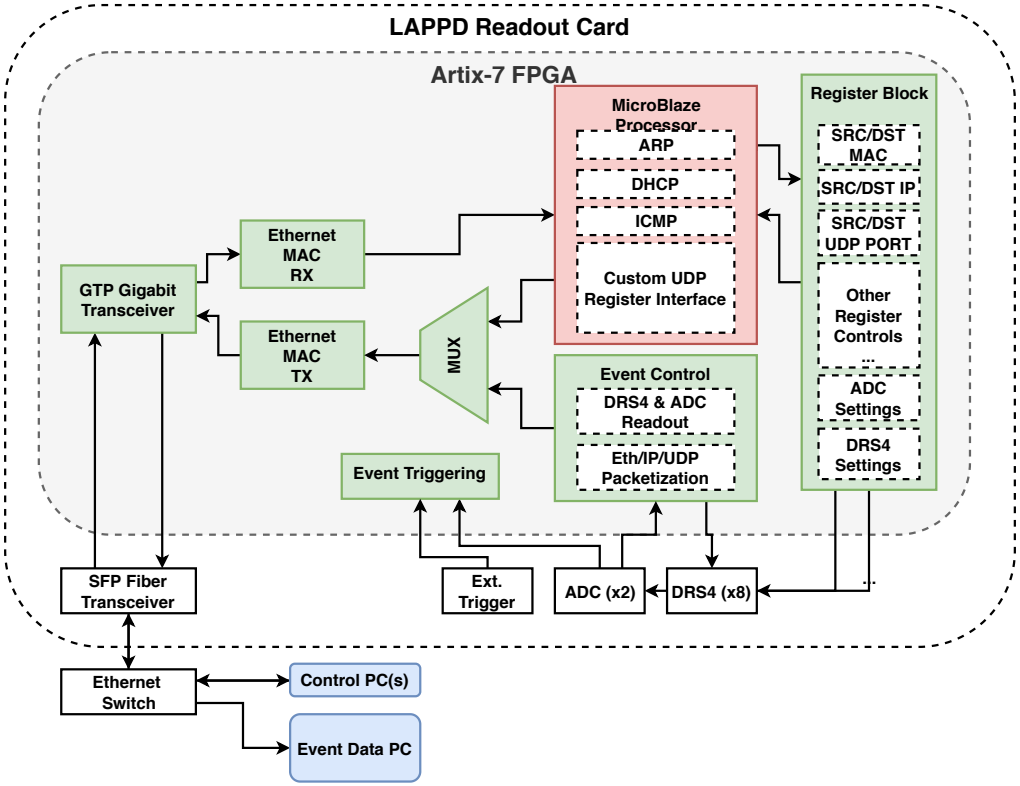


- Sampling with switched capacitor array of 1024 samples
- Sampling rate upto 5 GSPS
- Parallel read out of all channels
- Transparent mode for self triggering
- Region of interest readout mode which may significantly decreas readout lattency
- One channel in each DRS4 is connected to 100 MHz oscillator for time calibration

Firmware

- Control over DRS4 readout sequence
- Building of the event data and sending it to readout PC

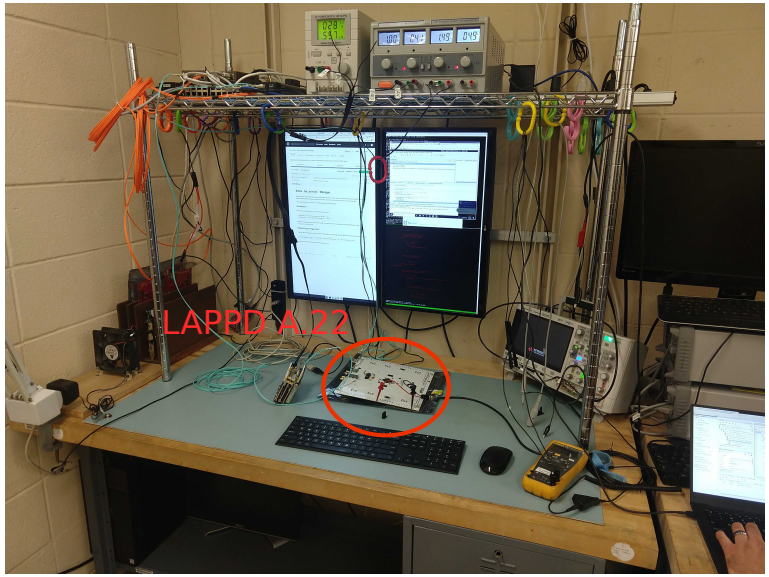
- Ethernet MAC inplemented in firmware
- Microblaze soft-core CPU allows implementation of ARP, DHCP and ICMP
- Asymmetric data flow: slow data channel for registers access and fast downstream at near full link bandwidth

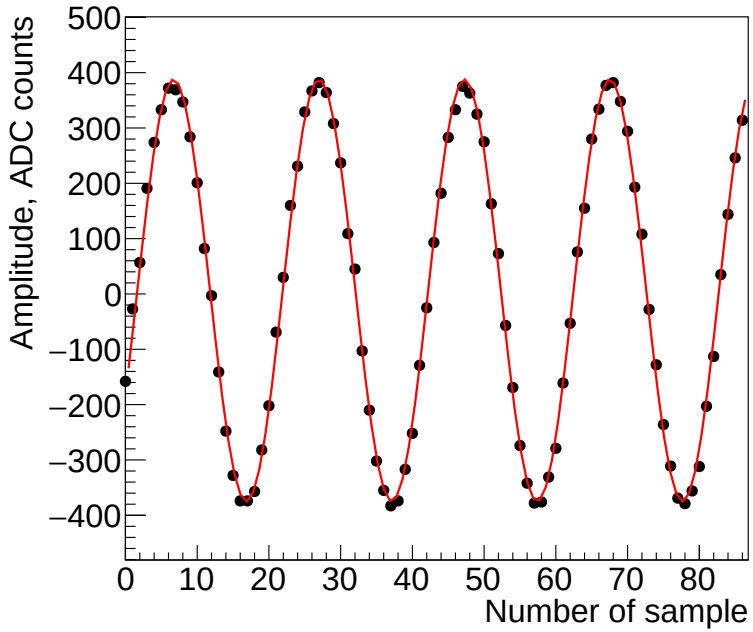


- UDP-based protocol for registers reads and writes
- Data stream from FPGA is multiplexed with slow data channel in fabric and and goes directly to Ethernet MAC TX

Firmware/hardware status

- Hardware is in the intence debugging phase. Because of minor bug in amplifiers baseline voltage very few channels are available after manual rework.
- Communication with readout PC works
- ADC control and deserialization works stably
- DRS4 control and readout sequence are implemented
- Readout of full waveform of 1024 samples takes about 120μs. May be improved to 60μs
- Simple waveform readout using registers interface
- DRS4 pedestals calibration procedure is implemented
- Read out sin wave for time calibration channel





Software

EEVEE
The Evolvable Embedded Vehicle for Execution of Experiments

Microblaze side: ARP, IP, DHCP, access to FPGA registers
PC side : basic functions library to communicate with the board

LAPPD control
LAPPD specific functions to set operational parameters of the board

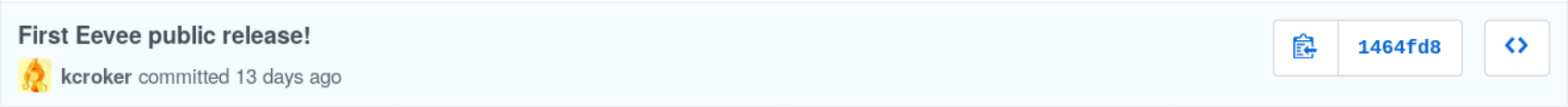
LAPPD digest
receive data stream, event unpacking and reconstruction

Visualization and control GUI

Open-source and extremely flexible software package is being developed.

https://github.com/kcroker/eevee

Software status



- Embedded Microblaze software has been developed. First public release was made about 2 weeks ago with full set of features: DHCP, automatic discovery of LAPPD boards connected, low-level library to communicate with the board.
- Development of back-end readout software is in progress. Event data format is developed and fixed. Event size for full waveform readout is about 100 kBytes. First version of unpacker is made.
- Data stream unpacking, pedestal substraction, reconstruction
- LAPPD control library with board specific functions to set parameters and control its operation is in progress.

Plans and schedule

- We are planning to implement full basic functionality in about one month from now.
- Minor bugs fix of the A.22 PCB related to amplifiers baseline voltages by November .
- Prepare the board to ship to Incom for testing on site in December.
- Fixing bugs in PCB by Ultralytics so complete board may be ordered from Ultralytics by the end of this year.

Conclusion

- Development of the universal highly integrated readout card for LAPPD is in progress.
- Significant part of the functionality is already implemented in the both firmware and software.
- We are planning to have fully functional prototype by the end of this year.
- Testing in PID prototypes next year?

Thank you for your attention!